LISTING OF CLAIMS:

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A self-supported III-V nitride semiconductor substrate having a substantially uniform carrier concentration distribution at least on its outermost surface, wherein said substrate has a carrier concentration of 1 x 10^{17} cm^{-3} or more, and wherein variations in the carrier concentration are within ± 25% in said outermost surface, said variations in the carrier concentration lying in a surface (in-plane) thereof.

2. (previously presented): The self-supported III-V nitride semiconductor substrate according to claim 1, wherein said substantially uniform carrier concentration distribution in a surface layer exists from the top surface to a depth of at least 10 μm.

Claims 3-9 canceled.

10. (previously presented): A III-V nitride semiconductor substrate having a substantially uniform carrier concentration distribution at least on its outermost surface, wherein said substrate has a carrier concentration of less than 1 x 10^{17} cm^{-3}, and wherein variations in the carrier concentration are within ± 100% in said outermost surface, said variations in the carrier concentration lying in a surface (in-plane) thereof.

Claims 11-12 canceled.

13. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein variations in the carrier concentration are not larger on-a top surface of said substrate than on a bottom surface of said substrate.

Claims 14-16 canceled.

17. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein a top surface of said substrate is polished.

18. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein a bottom surface of said substrate is polished.

19. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein said substrate has a thickness of 200 μm to 1 mm.

20. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein a top surface of said substrate is a (0001) group-III surface.

21. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein said substrate has a dislocation density lower on a top surface of said substrate than on a bottom surface of said substrate.

22. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein said substrate comprises a layer of GaN or A1GaN.

23. (currently amended): The III-V nitride semiconductor substrate according to claim ~~1~~ 1 or 2, wherein said III-V nitride semiconductor ~~crystal~~ substrate is doped with an impurity.

24. (previously presented): The III-V nitride semiconductor substrate according to claim 1 or 2, wherein at least part of said III-V nitride semiconductor substrate is grown by an HVPE method.

Claims 25-45 canceled.

46. (previously presented): The self-supported III-V nitride semiconductor substrate according to claim 10, wherein said substantially uniform carrier concentration distribution in a surface layer exists from the top surface to a depth of at least 10 μm.

47. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein variations in the carrier concentration are not larger on a top surface of said substrate than on a bottom surface of said substrate.

48. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein a top surface of said substrate is polished.

49. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein a bottom surface of said substrate is polished.

50. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein said substrate has a thickness of 200 μm to 1 mm.

51. (new): The III-V nitride semiconductor substrate according claim 10 or 46, wherein a top surface of said substrate is a (0001) group-Ill surface.

52. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein the said substrate has a dislocation density lower on a top surface of said substrate than on a bottom surface of said substrate.

53. (previously presented): The III-V nitride semiconductor substrate according to claim 10 or 46, wherein said substrate comprises a layer of GaN or AIGaN.

54. (previously presented): The III-V nitride semiconductor substrate 25 according to claim 10 or 46, wherein said III-V nitride semiconductor substrate is doped with an impurity.

55. (previously presented): The III-V nitride semiconductor substrate 25 according to claim 10 or 46, wherein said III-V nitride semiconductor substrate is doped with an impurity.